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SEAT No. :

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F.Y.B.Sc. (Computer Science)
ELECTRONIC SCIENCE
ELC-122: Basics of Computer Organization
(New 2019 Pattern) (CBCS) (Semester -II) (Paper-II)

[Time: 2 Hours]

[Max. Marks: 35]

Instructions to the candidates:

- 1) *Question 1 is compulsory.*
- 2) *Solve any three questions from Q2 to Q5.*
- 3) *Figures to the right indicate full marks.*
- 4) *Draw neat diagrams wherever necessary.*
- 5) *Questions 2 to 5 carry equal marks.*

Q.1) Solve any five of following.

[5]

- a) Write the full form for SR flip flop.
- b) What is virtual memory?
- c) How many address lines will be required to construct 4 MB of memory?
- d) Write the full form of CPU.
- e) Define register.
- f) Draw the logic symbol of D flop flip.

Q.2) A) Attempt the following:

- i) Draw and explain CPU (center processing unit) in detail. **[3]**
 - ii) Explain operation of ring counter with neat logic diagram. **[3]**
- B) Explain the concept of JK flip flop and draw its block diagram and truth table. **[4]****

P.T.O.

Q.3) A) Attempt the following:

i) Draw logic diagram of 3 bit PIPO shift register mode and explain its working. [3]

ii) Discuss in detail four (4) level memory of hierarchy. [3]

B) Draw neat block diagram of computer organization and explain it. [4]

Q.4) A) Attempt the following:

i) Explain concept of T flip flop in detail. [3]

ii) Explain the concept of memory stack organization with diagram. [3]

B) The number of reference made by CPU to memory (cache) is 100 and 80 times data was present in cache memory. How much will be the cache hit ratio and cache miss ratio. [4]

Q.5) Attempt any Four of the following:

[4 × 2½ = 10]

- Explain how JK flip flop can be converted into T flip flop.
- Compare Half duplex and Full duplex.
- Draw logic circuit diagram of three bits synchronous up counter.
- Write a short note on ROM.
- Compare CD and DVD (any three).
- How much time required paralleling in and serial out shift a 4 bit data in shift register operation at the clock frequency is 10 MHz.

