

Total No. of Questions : 5]

SEAT No. :

P1386

[Total No. of Pages : 2

[5623]-1006

F.Y. B.Sc. (Computer Science)

ELECTRONIC SCIENCE

ELC - 112 - Principles of Digital Electronics

(Semester - I) (New Pattern) (CBCS - 2019)

Time : 2 Hours]

[Max. Marks : 35


Instructions to the candidates:

- 1) Q.1 is compulsory.
- 2) Solve any three questions from Q.2 to Q.5.
- 3) Questions 2 to 5 carry equal marks.

Q1) Solve any five of the following :

[5 × 1 = 5]

a) $(1)_2 + (1)_2 + (1)_2 = (?)_2$.

b)  This gate is

- i) NAND.
- ii) NOR.
- iii) NOT.
- c) For a demultiplexer with 24 outputs the number of control inputs are _____.
- d) Find 1's complement of $(25)_{10}$.
- e) Define noise immunity.
- f) "Multiplexer circuit can be built by using OR - OR combinations of logic gates". State whether this statement is true or false.

Q2) a) i) Perform $(100)_{10} - (33)_{10}$ using 2's complement method. [3]

ii) Solve following equation using Boolean Algebra
 $Y = \bar{A}(B+C) + \bar{C} + AB$. [3]

b) Draw symbol and truth table of NAND and EX-OR Gate. [4]

P.T.O.

Q3) a) i) Convert the following expression into standard SOP form. [3]

$$Y = AB + \bar{B}C + \bar{C}$$

ii) Explain working of 3×4 matrix keyboard encoder. [3]

b) Draw and explain working of 1 : 4 demultiplexer. [4]

Q4) a) i) Simplify the following expression using K map [3]

$$Y = \bar{P}\bar{Q}R + \bar{P}Q\bar{R} + P\bar{Q}\bar{R} + \bar{P}Q\bar{R} + \bar{P}QR$$

ii) Draw logic circuit diagram for BCD to 7 segment converter. Give the logic levels to display digit '9' on common anode display. [3]

b) Perform the following [4]

i) $(11011)_{\text{gray}} = (?)_2$

ii) $(A5 \cdot D)_{16} = (?)_{10}$

Q5) Attempt any four of the following: [10]

a) Write a short note on BCD code.

b) State and prove De-Morgan's theorem.

c) Explain use of EX OR gate as parity generator.

d) Write the truth table for 3 bit binary to gray conversion.

e) Define following :

i) Fan in

ii) Fan out.

f) Explain working of half Adder.

