Total No	o. of Questions : 8]		SEAT No.:	
PD41	54		[Total	No. of Pages : 2
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	<u>-</u>	6402}-115		
	S.E. (Robotics & A	Automation Eng	gineering)	
	CONTROL SY	STEM ENGINE	ERING	
	(2019 Pattern) (Semester - IV)	(211509)	O .
		ŕ	1	
	½ Hours]			Max. Marks : 70
Instructi	ions to the candidates:		6	k
1)	Answers Q.1 or Q.2, Q.3 or Q.4,		1.8.	
2)	Neat aiagrams must be drawn v	•	12	
3)	Figures to the right side indica	•	1	
<i>4</i>)	Assume suitable data if necessa	ry.		
01)		1.11. 6.1.		ro1
Q1) a)	Explain Routh Hurwitz Sta		6 3	[9]
b)	If $G = K/S (S+6) (S+8)$ and	d H(S) = S+2. Cor	mment on sta	ability. [8]
	8.	OR O		
Q2) a)	What is stability? Explain stable system with location			d conditionally [9]
b)	i) The System with Ch	naracteristics Equa	ation $Q(S) =$	$S^3 + 2KS^2 +$
	(K + 2) S + 4 = 0 find	range of K for sta	bility	
	ii) Investigate the stabi			stics equation
	$Q(S) = S^5 + 5S^4 + 10$	$S_1^3 + 10S^2 + 5S + 1$	1 = 0	(
		3,		[4+4=8]
	0,6	•		
Q3) a)	Define phase margin and g	ain maroin Also di	raw a 40dh/d	ec line nassing
20) a)	through $w = 1.5$ db till $w = 1.5$		1411 4 TOGO/4	[8]

- - What is frequency domain analysis? Explain any one stability criteria used b) in frequency domain to check the stability of system. [9]

OR

- Draw the polar plot for (S) = 1 + as. **Q4**) a) [8]
 - Derive the expression for Resonant Frequency and Resonant Peak [9] b)
- Define PLC? What are the necessity of PLC? Give advantages and disadvantages of PLC.
 - State the sampling theorem explain the process of sampling and quantization with waveform. [9]

Explain digital control system in detail. Enlist its advantages and **Q6**) a) Applications. Explain the selection criteria used for PLC. [9] b) Enlist phase lead design steps using bode diagram with effects, **Q7**) a) advantages, disadvantages of phase lead compensation. [9] Explain the procedure to design of leg compensator using root locus.[9] b) OR Design a lead compensator for the system with open loop transfer **Q8**) a) function G(S) = 9/S(S+3) to meet following specifications. [11] Steady state error for ramp input be less than or equal to 0.05 Phase margin of at least 45 degree. b) Explain the Procedure to design of lead compensator using root locus.[7] S. As. 16.25 The hours of the control of the contro

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