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[5559]-207

S.E. (IT) (II Semester) EXAMINATION, 2019
PROCESSOR ARCHITECTURE AND INTERFACING
(2015 PATTERN)

Time : Two Hours

Maximum Marks : 50

- N.B. :—** (i) Answer Q. No. 1 or Q. No. 2, Q. No. 3 or Q. No. 4, Q. No. 5 or Q. No. 6, Q. No. 7 or Q. No. 8.
(ii) Neat diagrams must be drawn wherever necessary.
(iii) Figures to the right indicate full marks.

1. (A) With respect to the following points explain Assembler, Linker and Debugger : [6]
(1) Types of input and output files
(2) Command.
(B) Explain non-piplined bus cycle for WRITE operation with neat diagram. [6]

Or

2. (A) List any four addressing modes of 80386 microprocessor state difference between : [6]
(i) MOV EAX, 12345678 and MOV EAX, [12345678]
(ii) MOV EAX, ECX and MOV EAX, [ECX]
(B) Explain with neat diagram interprivilege level transfer using call gates. [6]

P.T.O.

3. (A) Explain in detail Page Directory Entry (PDE) and Page Table Entry (PTE). [6]

(B) Draw and explain block diagram of 8051 Microcontroller. [6]

Or

4. (A) Explain the following pins of 8051 : [6]

(i) TO

(ii) ALE

(iii) $\overline{\text{INT}}_1$

(B) Draw and explain format of TSS descriptor. [6]

5. (A) List operating modes of Timer of 8051 and explain any *two* of them. [7]

(B) Find the value to be loaded in TH₁ register to obtain the following baud rate : [6]

(i) 1200

(ii) 2400

(iii) 9600

Assume crystal frequency = 11.0592 MHz.

Or

6. (A) Find the value to restore in TH-TL pair to timer to generate square wave of 50 Hz and 2 kHz. Assume crystal frequency = 11.0592 MHz. [6]

(B) Explain significance of IP and IF register with format. [7]

Or

7. (A) Explain any *two* modes of operation of PPI 8255. [6]
(B) Explain ADC interfacing with 8051. Explain significance of any *two* interfacing control signals. [7]

Or

8. (A) How to configure port 1 and port 2 for two digit seven segment display ? Explain with diagram and instructions. [6]
(B) Explain External memory of size 64 kB (both program and data) interfacing with 8051. [7]