Total No. of Questions : 4]

SEAT No. :

PE-555

[Total No. of Pages : 2

[6578]-28
S.E. (IT) (Insem)
LOGIC DESIGN & COMPUTER ORGANIZATION
Information Technology
(2019 Pattern) (Semester - III) (214442)

Time : 1 Hour] *[Max. Marks : 30*

Instructions to the candidates:

1) ***Solve questions Q.1 or Q.2, Q.3 or Q.4***
2) ***Figures to the right indicate full marks.***
3) ***Neat diagrams must be drawn wherever necessary.***
4) ***Assume suitable data if necessary.***

UNIT - I

Q1) a) Explain following Characteristics of digital IC (TTL/CMOS): **[5]**

i) Fan in

ii) Fan Out

iii) Noise Margin

iv) Figure of merit

b) Represent $(+60)_{10}$ & $(-60)_{10}$ in - Sign-Magnitude form,1's complement form and 2's Complement form in 8- bit number format. **[5]**

c) Minimize the following function using K map in POS Form.

f (A, B,C, D) = πM(0,1,3,5,6,7,10,14,15) **[5]**

OR

Q2) a) Explain with help of suitable circuit diagram operation of 2-i/p CMOS NAND gate? **[5]**

b) Represent $(-0.8125)_{10}$ in Single precision and Double precision format. **[5]**

c) Convert the given expression into standard SOP form and simplify using K Map. **[5]**

Y=A + BC + ABC

P.T.O.

UNIT - II

Q3) a) Design and Implement 03 bit Binary to Gray Code convertor using basic gates. **[5]**

b) Draw the 9's Complement circuit using IC 7483. **[5]**

What are the rules of BCD Subtraction using 9's complement method.

c) Design Full Adder (FA) using IC 74153. **[5]**

OR

Q4) a) Design 03 bit Binary to Gray Code convertor circuit using Decoder IC 74138. **[5]**

b) Design and Implement 8:1 MUX using 4:1 MUX and Implement given function $F(X, Y,Z)=\Sigma m(1,3,4,7)$. **[5]**

c) State the rules of BCD Addition and Perform BCD Addition of $(75)_{BCD} + (35)_{BCD}$. **[5]**

❖❖❖