Total No. of Questions : 8]

SEAT No. :

PE4287

[Total No. of Pages : 2

[6582]-60R

S.E. (Information Technology)

LOGIC DESIGN AND COMPUTER ORGANIZATION

(2019 Pattern) (Semester - III) (214442)

Time : 2½ Hours] *[Max. Marks : 70*

Instructions to the candidates:

1) ***Answer Q.1 or Q.2, Q.3 or Q.4, Q.5 or Q.6, Q.7 or Q.8.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right indicate full marks.***
4) ***Assume suitable data, if necessary.***

Q1) a) Convert JK Flip Flop to T Flip-Flop. **[6]**

b) What is MOD counter? Design and draw logic diagram of Mod-82 counter using IC7490. **[7]**

c) Explain Shift Register and their types with applications. **[5]**

OR

Q2) a) Design 3-bit Asynchronous Down Counter using JK Flip Flop. **[6]**

b) What is the advantage of MS (Master Slave) Flip-Flop. Explain the working of MS JK Flip Flop in detail. **[6]**

c) What is the difference between asynchronous and synchronous counters? **[6]**

Q3) a) Describe the single bus organization of a CPU. What are some advantages and disadvantages of a single bus organization? **[6]**

b) What are the functions of Input output devices? What are the different types of I/O devices and how are they connected to a computer system? **[5]**

c) Explain the microprogrammed control unit. Write a microprogram of microinstructions for the following instruction ADD (R3) R1. **[6]**

OR

Q4) a) Explain in brief, various functional units of a computer system with a block diagram showing interconnection between them. **[6]**

b) With the help of neat diagram explain the Von Newman architecture. **[5]**

c) What is the function of control unit in a CPU? Compare Hardwired control Unit and Micro-programmed Control Unit. **[6]**

P.T.O.

Q5) a) Explain interrupt w.r.t. its purpose, types. Describe step by step, the interrupt handling procedure of microprocessors. **[7]**

b) Write about Taxonomy of Parallel Processor Architectures Organization. **[6]**

c) Explain SMP organization and its benefits. **[5]**

OR

Q6) a) What is meant by addressing mode? Mention different types of addressing modes? Explain any two addressing modes with suitable examples. **[6]**

b) Explain instruction pipelining? What are different types of pipelining hazards? **[6]**

c) What are the types of MIMD clusters? Discus in detail. **[6]**

Q7) a) Explain the Characteristics of Memory Systems and Memory Hierarchy. **[5]**

b) A set associative cache consists of 64 blocks divided in 4 block sets. The main memory contains 4096 blocks, each 128 words of 16 bit length. **[6]**

i) How many bits are there in main memory address?

ii) How many bits are there in cache memory addres (tag, set and word field)?

c) What are the different types of cache replacement policies? Explain with example. **[6]**

OR

Q8) a) Differentiate between SRAM, DRAM, and ROM based on their characteristics. **[5]**

b) Explain with state diagram - MESI protocol. **[6]**

c) Consider a fully associative cache with 8 lines (0-7). If the memory block requests are in the order 4, 3, 25, 8, 19, 6, 25, 8, 16, 35, 45, 22, 8, 3, 16, 25, 7. If LRU is used then which of the cache line will have memory block 7? Compute the Hit and Miss ratio. **[6]**