

Total No. of Questions : 4]

SEAT No. :

PC408

[Total No. of Pages : 1

[6359]-528

S.E. (Information Technology Engg.) (Insem)
LOGIC DESIGN & COMPUTER ORGANIZATION
(2019 Pattern) (Semester - III) (214442)

Time : 1 Hour]

[Max. Marks : 30

Instructions to the candidates:

- 1) Answer Q.1 or Q.2 and Q.3 or Q.4.
- 2) Neat diagrams must be drawn wherever necessary.
- 3) Figures to the right indicate full marks.
- 4) Assume suitable data, if necessary.

- Q1)** a) Draw and explain working of 02 input TTL NAND Gate. [5]
b) Represent $(+29)_{10}$ and $(-29)_{10}$ in sign magnitude form, 1's complement form & 2's complement form. [5]
c) Simplify using k-map.
 $F(A, B, C, D) = \sum m(0, 1, 5, 9, 10, 12, 14) + d(2, 4, 15)$. [5]

OR

- Q2)** a) Compare TTL & CMOS. [5]
b) Represent $(-140)_{10}$ in single Precision & Double precision format. [5]
c) Convert following equation in standard sop form and reduce using k-map.
 $F(A, B, C) = AB + BC + AC$. [5]

- Q3)** a) Perform conversion. [5]
i) $(100)_{10} = (?)_2 = (?)_{BCD} = (?)_{X5-3}$.
ii) $(11001110)_2 = (?)_{Gray}$.
b) Design Full Adder (FA) using DEMUX (1:8). [5]
c) Implement following Boolean expression using 3:8 line Decoder
 $F(P, Q, R) = \sum m(0, 1, 5, 7)$. [5]

OR

- Q4)** a) Design 03 bit Gray to Binary code converter using logic gates. [5]
b) Implement 4:1 mux using 2:1 mux. and Draw it's Truth table. [5]
c) Design Full Subtractor (FS) using IC 74138. [5]

