

Total No. of Questions : 8]

SEAT No. :

PB3652

[6261]-60

[Total No. of Pages : 2

S.E. (E.T.)

LOGIC DESIGN & COMPUTER ORGANIZATION

(2019 Pattern) (Semester-III) (214442)

Time : 2½ Hours]

[Max. Marks : 70

Instructions to the candidates:

- 1) Answer Q.1 or Q.2, Q.3 or Q.4, Q.5 or Q.6, Q.7 or Q.8.
- 2) Figures to the right indicates full marks.
- 3) Assume suitable data if necessary.

- Q1)** a) Differentiate between combinational Circuit and Sequential Circuit. [6]
b) Explain in detail the Conversion of D flip-flop to T flip-flop. [6]
c) Define Register. Explain various types of shift registers. [5]

OR

- Q2)** a) Draw the pin Configuration of IC 7476 and explain the function of Present and Clear pins. [6]
b) What is meant by race around condition? How race around condition can be eliminated? [6]
c) Define Modulus of Counter. Design MOD-81 counter using Decade Counter IC 7490. [5]

- Q3)** a) Explain following terms in brief i) ALU Signals ii) ALU Functions iii) ALU Types. [6]
b) What are the uses of Registers in a CPU? List typical Registers in a CPU. Write a short note on Flag register. [6]
c) What are interrupts? Explain with diagram what steps are carried out when they are present. [6]

OR

- Q4)** a) Write in brief about the Fetch cycle with operations and microinstructions carried out? [6]
b) Explain and Design basic structure of Von Neumann architecture. Write the difference between Harvard and Von Neumann architecture. [6]
c) Write a short note on following - Address Bus, Data Bus, Control Bus. [6]

P.T.O.

- Q5)** a) What is mean by Machine Instruction? Explain basic format of Machine instruction? What are the basic types of machine instructions? [6]
- b) What is meant by Multicore architecture? List the typical features of multicore intel core i7. [6]
- c) What is purpose of Interrupt? What are various types of Interrupts? [5]

OR

- Q6)** a) Explain interrupt handling. [6]
- b) Give the Taxonomy of Parallel Processor Architectures, with one line explanation of each type. [6]
- c) Identify the addressing mode in following instructions: [5]
- i) MOV R1, #0A2DH
- ii) MOV R1,R2
- iii) MOV R1, [R2]

- Q7)** a) Along with suitable diagram explain direct cache mapping technique.[6]
- b) What is DMA? Along with suitable diagram explain how DMA is used for data transfer. [6]
- c) Explain memory read cycle with timing diagram. [6]

OR

- Q8)** a) Compare : SRAM and DRAM. [6]
- b) Explain Cache Coherence. [6]
- c) Whata is Principle of Locality? Explain two types of Localities. [6]

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