Total No	. of Questions : 8] [6002]-166 S.E. (P.T.)	SEAT No. : [Total No. of Pages : 2
	LOGIC DESIGN & COMPUTER OR (2019 Pattern) (Semester - III)	
	/2 Hours] ons to the candidates:	(21 -1- 2) [Max. Marks : 70
1) 2)	Answer Q.1 or Q.2, Q.3 or Q.4, Q.5 or Q.6, Q.7 or Q.7	2.8.
3)	Figures to the right indicate full marks.	99°CO
Q1) a)	Define the following terms.	[8]
	i) Propagation Delay Time ii) Setup Time iii) Hold Time	
	iv) Maximum Clock Frequency	
b)	Draw and explain SR flip-flop using NAND	gate. [6]
c)	Convert T flip-flop to D flip-flop. OR	[4]
Q2) a)	Design MOD-45 counter using IC 7490.	[8]
b)	Draw and explain 4-bit serial-in serial-out sh	ift register using D _r FFs. [6]
c)	Differentiate between Latch and Flip Flop.	[4]
Q3) a)	Draw and explain Single bus organization of CPU?	of CPU State functions of [8]
b)	Explain sequence of events that occur in Fet diagram at each stage. OR	ch cycle symbolically with [9]
		P.T.O.

Q4)	a)	Draw the block diagram of Hardwired control unit. [8]		
	b)	Describe the functions of registers: IR, MBR, MAR, PC, Flag register.[9]		
Q 5)	a)	What are key characteristics of RISC & CISC. Compare RISC an CISC.	nd 9]	
	b)		ts 9]	
Q6)	a)	OR Draw and explain Cluster and Cluster Architectures. [9]	9]	
	b)	Explain symmetric multiprocessors(SMP) organization with features.[9]	•]]	
Q 7)	a)	What are the different algorithms and techniques used in managing cache		
			3]	
	b) 🖔	Explain Interrupt Driven I/O with a diagram. [9	9]	
		OR		
Q 8)		Draw & explain memory hierarchy structure? What is mean by a Principle of Locality. [9]		
	b)	Explain the memory write cycle with help of suitable timing diagram. [8	3]/	
		Explain the memory write cycle with help of suitable timing diagram. [8]	·	
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