Total No. of Questions : 8]

SEAT No. :

PA-1243

[Total No. of Pages : 2

[5925]-266
S.E. (IT)
LOGIC DESIGN & COMPUTER ORGANIZATION
(2019 Pattern) (Semester - III) (214442)

Time : 2½ Hours] *[Max. Marks : 70*

Instructions to the candidates:

1) ***Attempt Q.No.1 or Q.No.2, Q.No.3 or Q.No.4, Q.No.5 or Q.No.6, Q.No.7 or Q.No.8.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right indicate full marks.***
4) ***Assume suitable data, if necessary.***

Q1) a) Explain with a diagram, the conversion of J-K flip flop to D flip flop. **[9]**

b) Differentiate between Latch & flip-flop w.r.t. definition, operation, diagram of applications etc. **[9]**

OR

Q2) a) Design 3-bit synchronous down - counter using MS JK flip flop (IC 7476). (Pin numbers are not required) Draw only logic diagram. **[9]**

b) What is a shift register? State the types of shift registers with applications of each. **[9]**

Q3) a) Explain in brief, various functional units of a computer system with a block diagram showing interconnection between them. **[9]**

b) Write a short note on: PC, MAR, MBR, TR. **[8]**

OR

Q4) a) What is the function of control unit in a CPU? Draw block diagram of Hardwived control unit & explain its operation, pros & cons. **[9]**

b) Explain and draw basic structure of Harvard architecture. State the differences between Harvard and Von Neu mann architecture. **[8]**

Q5) a) What is meant by addressing mode? Explain all addressing modes with examples. **[9]**

b) Differentiate between RISC & CISC architecture. **[9]**

OR

P.T.O.

SPPU Question Papers
CEGP013091
49.248.216.238 06/02/2023 13:43:58 static-238

Q6) a) Explain instruction pipelining w.r.t. operation and speed up formula, achieved by pipelining. **[9]**

b) Explain interrupt w.r.t. its purpose, types. Describe step by step, the interrup handling procedure of microprocessors. **[9]**

Q7) a) Explain with examples the various cache replacement policies. Describe various cache write policies. **[9]**

b) Explain programmed controlled I/O with the help of flow chart. **[8]**

OR

Q8) a) Along with suitable diagram, explain set associative cache mapping technique. **[9]**

b) Explain memory read cycle with the help of suitable timing diagram. **[8]**

SPPUQuestionPapers.com
CEGP013091
49.248.216.238 06/02/2023 13:43:58 static-238