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Seat No.	
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[5459]-202

**S.E. (I.T.) (First Semester) EXAMINATION, 2018**  
**COMPUTER ORGANIZATION AND ARCHITECTURE**  
**(2015 PATTERN)**

**Time : Two Hours**

**Maximum Marks : 50**

- N.B. :-** (i) Answer *four* questions in all.  
(ii) Neat diagrams must be drawn wherever necessary.  
(iii) Figures to the right indicate full marks.  
(iv) Answer Q. Nos. 1 *or* 2, Q. Nos. 3 *or* 4, Q. Nos. 5 *or* 6, Q. Nos. 7 *or* 8.

1. (a) Multiply -7 and -3 using Booth's algorithm. [6]  
(b) Describe non-restoring division algorithm. [6]

*Or*

2. (a) What is an instruction cycle ? Explain with state diagram. [6]  
(b) Write a short note on register organization. [6]

3. (a) Draw and explain Hardwired Control Unit. [6]  
(b) Write control sequence by execution of the instruction ADD ( $R_1$ ),  $R_2$  for single bus architecture. [6]

*Or*

4. (a) A direct mapped cache has the following parameters : [6]  
Cache size = 1 K words, Block size = 128 words and main memory size = 64 K words. Specify the number of bits in TAG, BLOCK and WORDS in main memory address.

P.T.O.

- (b) Explain K-way set associate mapping techniques with its merits and demerits. [6]
5. (a) Describe MIPS architecture with diagram. [7]  
(b) Explain events of fetch cycle of MIPS pipeline. [6]
- Or*
6. (a) Explain types of hazards in pipeline architecture. [6]  
(b) Explain five stage pipelines with data paths and control path for MIPS architecture. [7]
7. (a) Explain closely coupled and loosely coupled microprocessor system. [7]  
(b) Write a short note on Multi-core architecture. [6]
- Or*
8. (a) Write short notes on : [6]  
(i) NUMA  
(ii) UMA  
(iii) CC-NUMA  
(b) Explain Flynn's taxonomy for multiple processor organization. [7]