Total No. of Questions : 8]

SEAT No. :

PF-12701

[Total No. of Pages : 2

[6627]-125
B.E. (Electronics & Telecommunication Engineering)
VLSI DESIGN & TECHNOLOGY
(2019 Pattern) (Semester -VII) (404182)

Time : 2½ Hours] *[Max. Marks : 70*

Instructions to the candidates :

1) ***Answer Q1 or Q2, Q3 or Q4, Q5 or Q6, Q7 or Q8.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right indicate full marks.***
4) ***Use of electronic pocket calculator is allowed.***
5) ***Assume suitable data, if necessary.***

Q1) a) Draw and explain the architecture of a CPLD. Mention its features and applications. **[9]**

b) Describe clock skew and clock jitter. Explain their effects on FPGA performance. **[8]**

OR

Q2) a) Explain the FPGA synthesis process with a suitable design example. **[9]**

b) Compare CPLD and FPGA in detail with respect to architecture, performance, and applications. **[8]**

Q3) a) Draw and explain the CMOS inverter and its voltage transfer characteristics. **[9]**

b) Discuss power dissipation mechanisms in CMOS circuits and explain Power Delay Product. **[9]**

OR

Q4) a) Explain the Latch-Up effect in CMOS circuits and discuss methods for its prevention. **[9]**

b) Design and explain a 2:1 multiplexer using CMOS transmission gates. **[9]**

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Q5) a) Discuss SPICE simulation and explain AC and DC analysis. **[9]**

b) Explain Lambda-based design rules and the significance of Design Rule Check. **[8]**

OR

Q6) a) Explain Antenna Effect and Electromigration Effect in VLSI circuits. **[9]**

b) Explain circuit extraction, ERC, and LVS verification techniques. **[8]**

Q7) a) Discuss different types of faults and fault models used in VLSI testing. **[9]**

b) Explain JTAG architecture and discuss the IEEE 1149.1 standard. **[9]**

OR

Q8) a) Explain the architecture and state diagram of the TAP Controller. **[9]**

b) Draw and explain the architecture of a Built-In Self-Test (BIST) system. **[9]**



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