Total No. of Questions : 8]

SEAT No. :

PE-2234

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B.E. (Electronics and Telecommunication Engineering)

VLSI DESIGN AND TECHNOLOGY

(2019 Pattern) (Semester - VII) (404182)

Time : 2½ Hours] *[Max. Marks : 70*

Instructions to the candidates:

1) ***Solve Q1 or Q2, Q3 or Q4, Q5 or Q6, Q7 or Q8.***
2) ***Assume suitable data, if necessary.***

Q1) a) Write the features of CPLD in detail and give it's applications. **[8]**

b) Draw and explain the architecture of FPGA & compare between CPLD and FPGA. **[10]**

OR

Q2) a) Draw and explain macrocell in detail. **[8]**

b) Draw and explain PLD design flow. **[10]**

Q3) a) Draw and explain CMOS Inverter schematic and it's voltage transfer characteristics. **[9]**

b) What are the merits of Transmission gate? Design 2:1 multiplexer using transmission gate. **[8]**

OR

Q4) a) Write short note on channel legth modulation. **[6]**

b) Write short note on Device siziry. **[6]**

c) Write short note on velocity saturation. **[5]**

Q5) a) What is DRC? Explain in detail rules in CMOS VLSI design? **[9]**

b) Draw stick diagram for Inverter, NAND and NOR gate. **[9]**

OR

Q6) a) Write short note on Design issues like Antenna Effect. **[6]**

b) Write short note on SPICE simulation. **[6]**

c) Write short note on Layout Vs schematic. **[6]**

P.T.O.

Q7) a) Explain the need for Design for Testability? Explain stuck-at-0 and stuck-at-1 faults with example. **[9]**

b) Write short note on **[8]**

i) JTAG

ii) Boundary scan

OR

Q8) a) What is the need of BIST? Explain typical BIST in detail. **[9]**

b) Draw the TAP controller state diagram and explain. **[8]**

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