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SEAT No. :

PE-231

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[6580]-594
B.E. (E & TC) (Insem.)
VLSI DESIGN AND TECHNOLOGY
(2019 Pattern) (Semester - VII) (404182)

Time : 1 Hour] *[Max. Marks : 30*

Instructions to the candidates:

1) ***Answer Q.1 or Q.2, Q.3 or Q.4.***
2) ***Neat diagrams must be drawn whenever necessary.***
3) ***Figures to the right indicate full marks.***
4) ***Assume any missing data if necessary.***

Q1) a) Write VHDL Code and its test bench of full adder. **[8]**

b) What is meant by concurrent and sequential statements in VHDL? Describe with examples. **[7]**

OR

Q2) a) Explain in detail digital design flow. **[8]**

b) Write VHDL code for 4:1 Mux using behavioral modeling style. Also write it test bench code. **[7]**

Q3) a) Differentiate following: **[8]**

i) Mealy and Moore Machine

ii) Fan In and Fan out

b) What is Clock Skew? What are techniques to minimize it? **[7]**

OR

Q4) a) Write short note on: **[8]**

i) Metastability

ii) Noise Margin

b) What are different signal integrity issues? How to minimize it. **[7]**

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