

Total No. of Questions : 8]

SEAT No. :

PC-2411

[Total No. of Pages : 2

[6354] - 529

B.E. (Electronics & Telecommunication Engineering)

VLSI DESIGN & Technology

(2019 Pattern) (Semester - VII) (404182)

Time : 2½ Hour]

[Max. Marks : 70

Instructions to the candidates:

- 1) *Neat diagrams must be drawn wherever necessary.*
- 2) *Figures to the right indicate full marks.*
- 3) *Use of electronic pocket calculator is allowed.*
- 4) *Assume suitable data, if necessary.*

Q1) a) Write short note on PLDs and explain each device involved in its classification in brief. **[8]**

b) Draw the block diagram of CPLD. **[9]**

Explain the following blocks with respect to CPLD :

- i) Macrocell
- ii) Product term Allocator:

OR

Q2) a) Draw block diagram of FPGA. **[9]**

Explain FPGA with respect to the following points:

- i) Configurable Logic Blocks
- ii) Programming Techniques

b) Compare FPGA with CPLD. **[8]**

Q3) a) Explain any two Non- Ideal Transistor I-V Effects. **[8]**

b) Draw CMOS logic for $Y=AB + C(D+E)$. Calculate W/L ratio for NMOS and PMOS as well as area needed on the chip. **[10]**

P.T.O.

OR

- Q4)** a) A CMOS logic is operating at 10 MHz and 3 V with the load of 100 pF. The static power dissipation is 100 μ W. Calculate the total power dissipation if the frequency is increased to 100 MHz. [6]
- b) Discuss need for transmission gate. Draw 4:1 Mux using TG. [6]
- c) Draw 2 input AND and OR gate using CMOS. [6]
- Q5)** a) Explain ASIC Design flow [6]
- b) Explain cell design specification [6]
- c) Draw stick diagram for CMOS Boolean Equation : $Y = \overline{A+B}$ [6]

OR

- Q6)** a) Explain LAMBDA rules used for CMOS layout Design [6]
- b) Write short note on Cross talk [6]
- c) Write SPICE code for CMOS inverter for AC analysis [6]

OR

- Q7)** a) What are the types of fault? Explain each in brief. [7]
- b) Explain the following terms with respect to testability: [10]
- Fault coverage
 - Fault Models
 - Observability
 - Controllability
 - Design for Testability

OR

- Q8)** a) What is need of BIST? Explain typical BIST in detail. [8]
- b) Draw and explain the state diagram of TAP controller. [9]

