Total No. of Questions : 4]

SEAT No. :

P5235

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[6188]-190
B.E. (E & TC) (Insem)
VLSI DESIGN AND TECHNOLOGY
(2019 Pattern) (Semester - VII) (Theory) (404182)

Time : 1 Hour] *[Max. Marks : 30*

Instructions to the candidates:

1) *Attempt Q.1 or Q.2 and Q.3 or Q.4.*
2) *Draw neat diagram's wherever necessary.*
3) *Figures to the right indicate full marks.*
4) *Assume suitable data, if necessary.*

Q1) a) Draw and explain design flow of VLSI. **[8]**

b) Write VHDL code for 8:1 mux using structural style of modeling. **[7]**

OR

Q2) a) Explain different modeling styles in VHDL. **[8]**

b) Write VHDL code for 4 - bit ALU to perform different eight operations. **[7]**

Q3) a) Explain and compare moore and mealy machine. **[8]**

b) Write short note on clock skew and clock jitter. **[7]**

OR

Q4) a) Write short note on noise margin. **[5]**

b) Explain signal integrity issues. **[5]**

c) Write short note on power distribution techniques. **[5]**

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