Total No. of Questions : 8]

SEAT No. :

P599

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[6004]-548

B.E. (Electronics & Telecommunication Engg.)
VLSI DESIGN & TECHNOLOGY
(2019 Pattern) (Semester - VII) (404182)

Time : 2½ Hours] *[Max. Marks : 70*

Instructions to the candidates:

1) ***Neat diagrams must be drawn wherever necessary.***
2) ***Figures to the right indicate full marks.***
3) ***Use of electronic pocket calculator is allowed.***
4) ***Assume suitable data, if necessary.***

Q1) a) Compare CPLD and FPGA on the basis of features, specifications and applications. **[6]**

b) Explain in brief classification of PLDs. **[6]**

c) Explain various stages of Synthesis in FPGA with suitable diagram. **[6]**

OR

Q2) a) Draw and explain the architecture of FPGA. Explain CLB in detail. **[10]**

b) Explain Clock Management Techniques in FPGA. **[8]**

Q3) a) Design CMOS logic for Y = AB + CD. Calculate W/L ratio for NMOS and PMOS area needed on chip. Find the total area. **[9]**

b) Discuss need for transmission gate. Draw 4 : 1 Mux using TG. **[8]**

OR

Q4) a) Draw CMOS logic for 2 input NAND gate. Explain its working and draw its stick diagram. **[9]**

b) Explain the working of CMOS inverter with the help of Voltage Transfer curve. **[8]**

Q5) a) Draw and explain ASIC design flow. **[6]**

b) Discuss Lambda rules with diagram? (Any 6 rules) **[6]**

c) What is stick diagram? Draw Stick diagram of CMOS Inverter. **[6]**

OR

P.T.O.

Q6) Write short note on : **[18]**

a) Antenna Effect.

b) Crosstalk.

c) Electro migration.

Q7) a) Explain need of Design for Testability. **[8]**

b) Explain Stack at Fault models in brief. **[9]**

OR

Q8) a) Write short note on Built in Self-Test. **[8]**

b) Write short note on Boundary Scan Method for testing. **[9]**

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