

Total No. of Questions :6]

SEAT No. :

P228

Oct./BE/Insem. - 544

[Total No. of Pages : 1

B. E. (E & TC)

**VLSI DESIGN AND TECHNOLOGY
(2015 Course) (Semester - I) (404181)**

Time : 1 Hour]

[Max. Marks : 30]

Instructions to the candidates:

- 1) Solve Q1. or Q2, Q3 or Q4, Q5 or Q6.
- 2) Neat diagrams must be drawn wherever necessary.
- 3) Black figures to the right indicate full marks.
- 4) Assume suitable data, if necessary.

- Q1)** a) Explain signal and variable difference in VHDL [6]
b) Explain different types of data types in VHDL [4]
- OR
- Q2)** a) Explain function and procedure with example. [6]
b) Explain any two concurrent statements in VHDL with syntax. [4]
- Q3)** a) Explain what is metastability and solution for it. [6]
b) Explain clock jitter & clock skew. [4]
- OR
- Q4)** a) Explain power optimization techniques. [6]
b) List and explain briefly signal integrity issues. [4]
- Q5)** a) Draw and explain microcell in CPLD. [6]
b) Explain interconnect routing technique. [4]
- OR
- Q6)** a) Explain FPGA Synthesis and implementation. [6]
b) Explain features of CPLD. [4]

