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SEAT No. :

P5784

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**B.E./Insem/Oct-546**  
**B.E. (E & T.C) (Semester - I)**  
**VLSI Design and Technology**  
**(2015 Pattern)**

*Time : 1 Hour]*

*[Max. Marks : 30*

*Instructions to the candidates:*

- 1) *All questions are compulsory.*
- 2) *Neat diagrams must be drawn wherever necessary.*

**Q1)** a) Draw HDL design flow and explain. [6]

b) Explain various VHDL operators. [4]

OR

**Q2)** a) Explain sequential statements in VHDL with syntax. [6]

b) Write VHDL code for 1 bit full adder. [4]

**Q3)** a) Explain clock skew and any one clock distribution technique. [6]

b) Write short note on signal integrity issues. [4]

OR

**Q4)** a) Write short note on metastability and synchronizers. [6]

b) Write note on supply and ground bounce. [4]

**Q5)** a) Draw and explain CPLD architecture. [6]

b) Explain any four features of FPGA. [4]

OR

**Q6)** a) Draw and explain FPGACLB architecture. [6]

b) Write four differences between CPLD and FPGA. [4]

