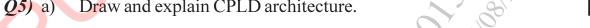
Total No	o. of Questions : 6] SEAT No. :	
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13/04	B.E/Insem/Oct-546	,
	B.E. (E & T.C) (Semester - I)	
	VLSI Design and Technology	
	(2015 Pattern)	
Time: 1		s : 30
	tions to the candidates:	
1)	All questions are compulsory.	
2)	Neat diagrams must be drawn wherever necessary.	
<b>Q1)</b> a)	Draw HDL design flow and explain.	[6]
b)	Explain various VHDL operators.	[4]
	OR	
<b>Q2)</b> a)	Explain sequential statements in VHDL with syntax.	[6]
b)	Write VHDL code for 1 bit full adder.	[4]
<b>Q3)</b> a)	Explain clock skew and any one clock distribution technique.	[6]
b)	Write short note on signal integrity issues.	[4]
	OR	X
<b>Q4</b> ) a)	Write short note on metastability and synchronizers.	[6]
b)	Write note on supply and ground bounce.	[4]
,	9,30	- 1
<b>Q5</b> (a)	Draw and explain CPLD architecture	[6]



b) Explain any four features of FPGA. [4]

OR

**Q6)** a) Draw and explain FPGACLB architecture. [6]

b) Write four differences between CPLD and FPGA. [4]

