Total No. of Questions : 10]

SEAT No. :

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S.E. Electronics and Communication Engineering (Advanced Communication Technology)

PCC 253-ECA: DIGITAL CIRCUITS

(2024 Pattern) (Semester - IV)

Time : 2½ Hours] *[Max. Marks : 70*

Instructions to the candidates:

1) ***Solve Q1 or Q2, Q3 or Q4, Q5 or Q6, Q7 or Q8, Q9 or Q10.***
2) ***Neat diagrams should be drawn wherever necessary.***
3) ***Assume suitable data if necessary.***

Q1) a) Implement the following function using 8:1 multiplexer f (A,B,C) = Σm (2, 4, 5, 7, 10. 14). **[8]**

b) Design the full adder using logic gates. **[6]**

OR

Q2) a) Implement the following Boolean function using a 3:8 decoder and external gates. f (A,B,C) = Σm(2, 4, 5, 7) **[8]**

b) Implement the full subtractor using a 1:8 De-multiplexer. **[6]**

Q3) a) Design a sequence generator using TFFs. **[8]**

$0 \rightarrow 1 \rightarrow 4 \rightarrow 7 \rightarrow 2$

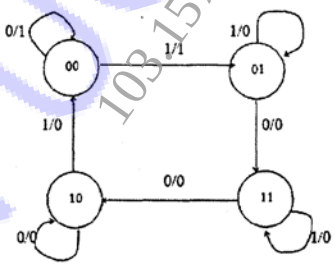
b) Explain the working of JK flipflop with neat block diagram and truth table. **[6]**

OR

Q4) a) Design a circuit to generate the following sequence using D flipflop. 1011. **[8]**

b) With the neat diagram, explain the working operation of 4-bit SISO. **[6]**

Q5) a) Design the clocked sequential circuit for the state diagram using T flip flop. **[8]**



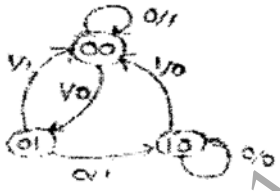
b) Design a sequence detector to detect a sequence 111 using D FF (Use Mealy machine). **[6]**

OR

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Q6) a) Design the sequential circuit for the given state diagram using T flipflop. **[8]**



b) Draw ASM chart for 2-bit binary counter having one enable line E such that: E=1 Count Enable and E=0, Count Disable. **[6]**

Q7) a) Draw ASM chart for the circuit that has control input C, clock and outputs x, y, z. **[8]**

i) If C=1 on every rising edge of the clock code on output x, y and z changes from: 000 → 010 → 100 → 110 → 000 and repeats.

ii) If C=0 then the circuit holds the present state.

b) Draw a combinational circuit for a PLA with 3 inputs, 3 product terms and 2 outputs. **[6]**

OR

Q8) a) Classify and explain the characteristics of memories. **[8]**

b) Compare different Logic Families: RTL, DTL. TTL and ECL. **[6]**

Q9) a) Explain : Counters ring counters and ripple counters. **[8]**

b) Explain: Programmable logic devices PAL, PLA. **[6]**

OR

Q10)a) List out the features and typical specifications of FPGA and CPLD. **[8]**

b) Draw and explain CMOS inverter. **[6]**

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