Total No. of Questions : 8]

SEAT No. :

PE4256

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S.E. (Electronics/E & TC) (Electronics & Computer Engg.Electronics (VLSI Design & Tech.)/E.C(A.C.T.))

DIGITAL CIRCUITS

(2019 Pattern) (Semester - III) (204182)

Time : 2½ Hours] *[Max. Marks : 70*

Instructions to the candidates:

1) ***Solve Q1 or Q2, Q3 or Q4, Q5 or Q6, Q7 or Q8.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right indicate full marks.***

Q1) a) Design of one-bit magnitude comparator. **[6]**

b) Implement the following expression using single 8 : 1 multiplexer **[6]**

$$Y = \sum m(0,1,2,5,7,8,9,14,15)$$

c) Write a short note on Look ahead carry generator. **[6]**

OR

Q2) a) Design of 3 bit even parity generator. **[6]**

b) Implement the following function using 1 : 8 De-multiplexer. **[6]**

F1(A,B,C) = Σ*m*(0,3,7)

F2(A,B,C) = Σ*m*(1,2,5)

F3(A,B,C) = Σ*m*(1,3,6)

c) Write a short note on ALU. **[6]**

Q3) a) Define the following terms as applied to flip-flop. **[6]**

i) Set up time

ii) Hold time

iii) Propagation Delays

b) Perform the JK flip-flop to D flip-flop conversion. **[6]**

c) Design and implement a MOD 6 asynchronous counter IC 7490. **[5]**

OR

P.T.O.

Q4) a) Design a sequence generator to generate sequence 11001 using shift register. **[6]**

b) Design and implement a MOD 4 synchronous counter using D flipflop. **[6]**

c) Explain the various modes of shift Register. **[5]**

Q5) a) Design sequence detector to detect a sequence 101... using D flip-flops. Use mealy machine. **[9]**

b) Draw an ASM chart for a 2-bit binary counter having enable line E such that E=1 (counting enabled) and E = 0 (hold present count). **[8]**

OR

Q6) a) Design sequence detector to detect a sequence 110... using T flip-flops. Use mealy machine. **[9]**

b) Draw an ASM chart and state table for a 2-bit up-down counter having mode control input : **[8]**

M = 1 : Up counting

M = 0 : Down counting

The circuit should generate a output 1 whenever count becomes minimum or maximum.

Q7) a) Compare between PROM, PAL, PLA **[6]**

b) Design following functions using PLA. **[6]**

$F_1 = \sum m(1,3,5)\ F_2 = \sum m(5,6,7)$

Implement the circuit with a PLA having 3 inputs, 3 product terms and 2 output.

c) Draw and explain the architecture of CPLD. **[6]**

OR

Q8) a) Draw a neat diagram of one cell of staticRAM and explain its working. **[6]**

b) Design following functions using PLA : **[6]**

$F_1 = \sum m(3,5,7)\ F_2 = \sum m(4,5,7)$

c) Draw and explain the architecture of FPGA. **[6]**