Total No. of Questions : 8]

SEAT No. :

P9102

[Total No. of Pages : 2

[6179]-227

S.E. (Electronics / E & TC / Computer)

DIGITAL CIRCUITS

(2019 Pattern) (Semester-III) (204182)

Time : 2½ Hours] *[Max. Marks : 70*

Instructions to the candidates:

1) ***Solve Q.No.1 or Q.No.2, Q.No.3 or Q.No.4, Q.No.5 or Q.No.6, Q.No.7 or Q.No.8.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right indicate full marks.***
4) ***Use of Calculator is allowed.***
5) ***Assume suitable data, if necessary.***

Q1) a) Explain binary subtraction using l's compliment and two's compliment method with example. **[6]**

b) Design and explain 3-bit parity generator circuit. **[6]**

c) Implement 1:8 demux using 1:4 demux. **[6]**

OR

Q2) a) Design and explain 2-bit comparator circuit using logic gates. **[6]**

b) Implement 16:1 Mux using 4:1 Mux. **[6]**

c) Explain Look ahead carry generator circuit. **[6]**

Q3) a) Explain working of SR Flip flop with neat Block diagram and truth table. **[6]**

b) Convert JK flip flop into D flip flop. **[6]**

c) Design and implement 2-bit synchronous counter using T flip flop. **[5]**

OR

Q4) a) Explain working of JK Flip flop with neat Block diagram and truth table. **[6]**

b) Convert SR flip flop into T flip flop. **[6]**

c) Write short note on Shift registers. **[5]**

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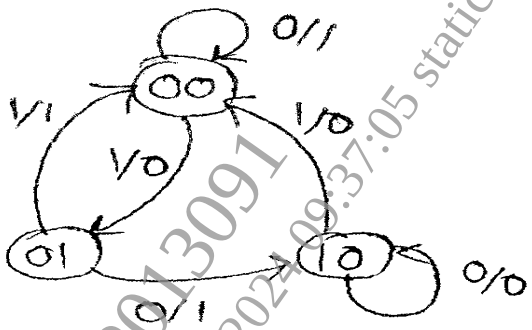
Q5) a) Design the sequential circuit for the given state diagram using T flip flop. **[9]**



b) Design and implement circuit using D flip flop to detect the following binary sequence 110. **[8]**

Q6) a) Draw ASM chart for 2 bit binary counter having enable line E such that: E=1, Count Enable and E=0, Count Disable. **[9]**

b) Write short note on state reduction with suitable example. **[8]**

Q7) a) Explain the block diagram of memory unit? **[9]**

b) Explain FPGA architecture. **[9]**

OR

Q8) a) Design and implement Full Subtractor using PAL? **[9]**

b) Explain CPLD architecture. **[9]**

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