[6002]-112

S.E. (Electronics/ E&T.C)
ELECTRONIC CIRCUITS.
(2019 Pattern) (Semester-III) (204181)

Time : 2½ Hours]   *[Max. Marks : 70*

Instructions to the candidates:

1) Answer Q.1 or Q.2, Q.3 or Q.4, Q.5 or Q.6, Q.7 or Q.8.
2) Figure to the right indicate full marks.
3) Neat diagrams must be drawn wherever necessary.
4) Assume suitable additional data, if necessory.
5) Use of non-programmable calculator is allowed.

Q1) a) Draw block diagram of regulated power supply and explain the function of each block? **[6]**

b) With the help of neat diagram explain buck-boost converter? **[6]**

c) Draw and explain low dropout regulator? **[6]**

OR

Q2) a) Design a regulated power supply using LM 317 for output voltage gv and 15v IAdj=100 *u*A. **[6]**

b) Explain the working of SMPS with neat diagram? **[6]**

c) Compare regulated and unregulated power supply? **[6]**

Q3) a) List all parameter's of op-amp. Explain any four in brief ? **[6]**

b) Explain significance of negative feed back, in op-amp amplifier? **[5]**

c) A dualt input balanced output differential amplifier has following specification Rc=2.7KΩ, RE=4.5kΩ, $\pm$ VCC=$\pm$10v, β=100; VBE=0.7V; re=26.34Ω calculate **[6]**

i) Voltage gain (Ad)

ii) Rin

iii) Ro

OR

Q4) a) Draw block diagram of op-amp and explain each block? **[6]**

b) Compare inverting and non-inverting configuration of op-amp with following parameters:

i) Feedbock Type

ii) Ri

iii) Gain

iv) Bandwith **[5]**

P.T.O.

c) Determine the Q point for dual input and balanced output differential amplifier with RC=RE=65KΩ and supply voltage $\pm$ 15V assume suitable data. **[6]**

Q5) a) Draw an inverting summing amplifier with three input and derive expression for the output voltage Vo= – (Va+Vb+Vc) **[6]**

b) Design a practical Integrator with input Signal of 1.5 vpp and cut off frequency of 3KHz for DC voltage gain of 10. **[6]**

c) Draw circuit diagram of 30p-amp Intrumentation amplifier and write its o/p equation? **[6]**

OR

Q6) a) With the help of neat diagram explain working of symmetrical schmitt trigger? **[6]**

b) Design a square wave generater using op-amp for frequency 1KHz to 10 KHz with 50 % duty cycle. draw diagram with component value. **[6]**

c) Explain practical differentiator circuit with neat diagram? list limitations of ideal differentiator? **[6]**

Q7) a) Explain voltage to current converter with floating load? **[6]**

b) Determine the output voltage produced by 4 bit R-2R ladder DAC with Vret=5v for bit sequence i) 0110 ii) 1101 **[5]**

c) Explain working of flash ADC in details. **[6]**

OR

Q8) a) Define terms. **[6]**
    i) Lock range
    ii) Capture range.
    iii) Pull in time
    iv) Free running frequency.

b) With the neat diagram explain working of weighted resistor DAC? **[6]**

c) Find the digital output of an ADC having t1=83.33 Msec and VR=100 mv for an input voltage. of +100mV. The clock frequency is kHz **[5]**

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