Total No. of Questions : 8]

SEAT No. :

P1486

[Total No. of Pages : 2

[6002]-113

S.E. (Electronics/Electronics & Computer/E & TC)

DIGITAL CIRCUITS

(2019 Pattern) (Semester - III) (204182)

Time : 2½Hours] *[Max. Marks : 70*

Instructions to the candidates:

1) *Answer Q.No.1 or Q.No.2, Q.No.3 or Q.No.4, Q.No.5 or Q.No.6, Q.No.7 or Q.No.8.*
2) *Neat diagrams must be drwan wherever necessary.*
3) *Figures to the right indicates full marks.*

Q1) a) Explain the working of a half-adder? Draw its logic diagram. **[7]**

b) Implement the full subtractor using a 1 : 8 demultiplexer. **[5]**

c) Implement the following function using multiplexer.
$f(A,B,C) = \sum m\ (0, 2, 4, 6)$. **[5]**

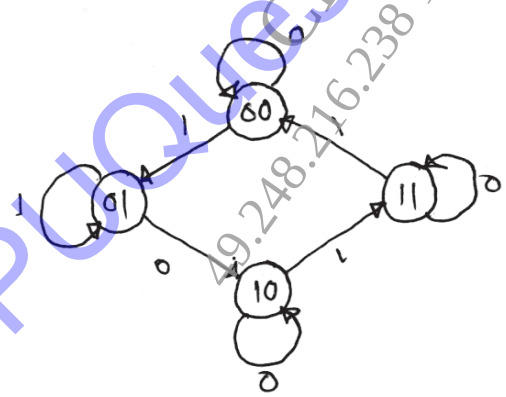
OR

Q2) a) Draw the logic diagram of full-adder and its truth table. **[7]**

b) Implement a full-adder using Demultiplexer. **[5]**

c) Implement the given logic function using a 4 : 1 multiplexer.
$f(A,B,C) = \sum m\ (0, 2, 4, 6)$. **[5]**

Q3) a) For the state diagram shown in figure, obtain the state table and design the circuit using minimum number of J = K flip - flops. **[8]**



b) Explain the function of a shift register. Give its application. **[5]**

c) Explain with truth table the working of clocked RS flip-flop. **[5]**

OR

Q4) a) Design a sequence generator using T FFs $0 \rightarrow 1 \rightarrow 7 \rightarrow 4 \rightarrow 2$. **[8]**

b) Explain the types of shift register. **[5]**

c) Explain with diagram the working of D type Flip-flop. Give its truth table. **[5]**

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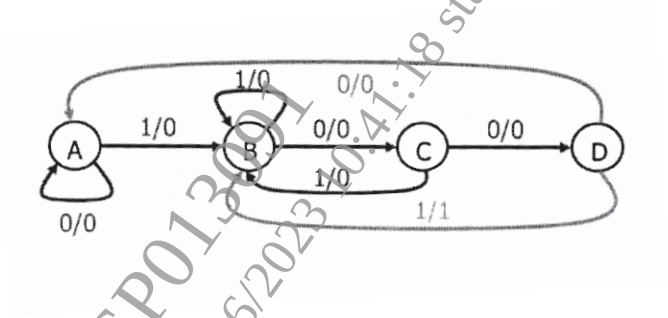
Q5) a) Design the clocked sequential circuit for the state diagram using JK flip flop. **[9]**



b) Draw ASM chart for a 2 bit up-down counter having mode control input M. **[8]**
M=1 Up counter.
M = 0 Down Center.

OR

Q6) a) Design a sequential circuit using Mealy machine for detecting the sequence.....1001.....Use Jk Flip-flop. **[9]**

b) Explain in short: **[8]**
i) State Diagram.
ii) ASM chart.

Q7) a) Explain the classification of memories based on their principle of operation. **[8]**

b) Write a short note on concept of PLA and PAL. **[10]**

OR

Q8) a) Explain with circuit diagram the dynamic MOS memory. **[8]**

b) A combinational circuit defined by the function. **[10]**
$F_1(A, B, C) = \sum (3, 5, 6, 7)$ and $F_2(A, B, C) = \sum (0, 2, 4, 7)$
Implement the circuit with PLA having 3 inputs, 3 products terms and 2 out puts.

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