[5931]-8

S.E. (Electronics/E&TC/Electronics & Computer)

DIGITAL CIRCUITS

(2019 Pattern) (Semester - I) (204182)

Time : 1 Hour]

[Max. Marks : 30

Instructions to the candidates:

1) *Answer Q.1 or Q.2, Q.3 or Q.4, Q.5 or Q.6.*

2) *Figures to the right indicate full marks.*

3) *Neat diagrams must be drawn wherever necessary.*

4) *Use of non-programmable calculator allowed.*

5) *Assume suitable data, if necessary.*

Q1) a) Explain the following characteristics of digital IC's. **[6]**

   i) Figure of Merit

   ii) Propagation delay

   iii) V_{IH} and V_{OH}

   b) Draw and explain the working of CMOS Inverter. **[4]**

OR

Q2) a) Draw and explain the working of 2-input TTL NAND gate. List advantages of Totem Pole. **[6]**

   b) Explain the following characteristics of digital IC's. **[4]**

   i) Noise Margin

   ii) Fan out and fan in

Q3) a) Design full adder using logic gates. **[4]**

   b) Minimize the following expression using K-map and implement using logic gates : $Y = \Sigma m (1, 3, 5, 9, 11, 13)$. **[6]**

OR

Q4) a) Design 3-bit Gray code to Binary converter. **[6]**

b) Design full subtractor using logic gates. **[4]**

Q5) a) Minimize the following function using K-map and implement it using only NAND gates. $F(P, Q, R, S) = \Sigma m\ (4, 5, 6, 7, 8, 12) + d\ (1, 2, 3, 9, 11, 14)$ **[6]**

b) Compare TTL and CMOS logic families. **[4]**

OR

Q6) a) Explain the current parameters in TTL logic. **[4]**

b) Minimize the following function using Quine Mc Clusky method. $F(A, B, C, D) = \Sigma \pi\ (0, 3, 5, 7, 12, 15) + d\ (2, 9)$. **[6]**

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