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[5668]-135

S.E. (E&TC/Electronics) (First Semester) EXAMINATION, 2019

DIGITAL ELECTRONICS

(2015 PATTERN)

Time : Two Hours

Maximum Marks : 50

- N.B. :-**
- (i) Answer Q. No. 1 or Q. No. 2, Q. No. 3 or Q. No. 4, Q. No. 5 or Q. No. 6 and Q. No. 7 or Q. No. 8.
 - (ii) Figures to the right indicate full marks.
 - (iii) Neat diagram must be drawn wherever necessary.
 - (iv) Use of non-programmable calculator is allowed.
 - (v) Assume suitable data, if necessary.

1. (a) Draw and explain Master-Slave JK flip-flop. [6]
(b) Design Mod 8 synchronous counter using T flip-flop. [6]

Or

2. (a) Convert SR flip-flop to JK flip-flop. [6]
(b) Implement a full adder using 8 : 1 multiplexer. [6]

3. (a) Design the sequence generator using JK flip-flop
 $0 \rightarrow 2 \rightarrow 4 \rightarrow 6 \rightarrow 0$ [6]
(b) Explain working of 2 input TTL Nand gate with totem pole. [6]

P.T.O.

Or

4. (a) Compare TTL and CMOS logic family. [6]
(b) Draw circuit diagram of 3-bit SIPO shift register using D flip-flop. Explain its working. [6]

5. (a) A combinational circuit defined by $f_1 = m(0, 3, 4, 7)$ and $f_2 = m(1, 2, 5, 7)$. Implement using PLA. [6]
(b) Compare SRAM and DRAM. [3]
(c) Explain PAL with the help of neat a diagram. [4]

Or

6. (a) Implement the following using PAL
$$F(A, B, C, D) = \sum m(0, 1, 3, 15)$$
 [6]
(b) Draw and explain structural diagram of CPLD. [4]
(c) Compare CPLD with FPGA. [3]

7. (a) Write a program for subtraction of 8-bit binary numbers. [3]
(b) Explain any *two* addressing modes of 8051. [4]
(c) Explain the following instructions with examples : [6]
(i) CJNE
(ii) SUBB A, R0
(iii) JMP @ A + DPTR
(iv) LCALL code addr

Or

8. (a) Draw the pin diagram of 8051 microcontroller and explain its port structure. [6]
- (b) Explain the function of the following pins of 8051 : [3]
- (i) EA
 - (ii) $\overline{\text{PSEN}}$
 - (iii) RST
- (c) List the features of 8051. [4]