

Total No. of Questions : 8]

SEAT No. :

PD-5230

[Total No. of Pages : 3

[6402]-30

S.E. (Electronics and Computer Engineering)

ELECTRONIC CIRCUITS

(2019 Pattern) (Semester - III) (204202)

Time : 2½ Hours]

[Max. Marks : 70

Instructions to the candidates :

- 1) Answer Q1 or Q2, Q3 or Q4, Q5 or Q6, Q7 or Q8.
- 2) Neat diagrams must be drawn wherever necessary.
- 3) Figures to the right side indicate full marks.
- 4) Use of Calculator is allowed.
- 5) Assume Suitable data if necessary

Q1) a) Design an adjustable voltage regulator using LM317 for output voltage 15V and output current 0.5 Amp with necessary connection diagrams. Assume $R_1=240\Omega$, $I_{adj}=100\mu A$. [6]

b) Draw and explain buck type switching regulator with necessary waveforms. [6]

c) Draw and explain the concept of current boosting in adjustable three terminal voltage regulator. [6]

OR

Q2) a) What is need of DC regulator supply? Enlist the performance parameters of voltage regulator with ideal values. [6]

b) With the help of a neat block diagram explain the operation of three terminals an adjustable voltage regulator. [6]

c) What is LDO regulator? Explain in its operation. Enlist the advantages of LDO. [6]

Q3) a) Write short note on current mirror circuit. [6]

b) An emitter biased Dual input balanced output differential amplifier has the following specifications : $V_{CC} = \pm 12 V$, $R_{C1} = R_{C2} = 2k\Omega$ and $R_E = 5k\Omega$, $\beta = 100$ & $V_{BE} = 0.7V$. [6]

Calculate :

- i) Voltage Gain (A_d)
 - ii) Input Resistance (R_i)
 - iii) Output Resistance (R_o)
- c)** What is significance of 1. Slew rate, 2. CMRR and 3. Gain bandwidth product in Op Amp. [6]

P.T.O.

OR

- Q4)** a) Explain the concept of virtual short and virtual ground with relevant diagrams. [6]
- b) A dual input balanced output differential amplifier has following specification $R_B = 2.7k\Omega$, $R_E = 4.5k\Omega$, $\pm V_{CC} = \pm 10V$, $\beta = 100$; $V_{BE} = 0.7V$; $r_e = 26.34\Omega$. [6]
- calculate
- i) Voltage gain (A_d)
- ii) R_{in}
- iii) R_o
- c) Why level shifter circuit is required in Op Amp? Explain level shifter circuit used in Op Amp. [6]

- Q5)** a) Design a practical differentiator circuit to differentiate an input signal that values in the frequency 10 Hz to 1 kHz. Assume $f_a = 10$ fb and $C_1 = 1\mu f$. [6]
- b) Draw and explain the following circuits using Op Amp [6]
- i) Difference amplifier
- ii) Voltage follower.
- c) Draw and explain working of symmetrical Schmitt trigger, with suitable waveform and hysteresis loop. [6]

OR

- Q6)** a) Draw and explain instrumentation amplifier using three Op-amps. Derive the expression for output voltage. [6]
- b) Design a practical integrator with input signal of $2V_{pp}$ and cut off frequency of 2.5 kHz for DC voltage gain of 10. [6]
- c) Explain practical differentiator circuit with neat diagram? List limitations of ideal differentiator? [6]

- Q7) a)** Determine the output voltage produced by 4 bit R-2R ladder DAC with $V_{ref} = 5\text{ V}$ for input bit sequence [5]
- i) 0110
 - ii) 1101
 - iii) 1000
- b) Draw 3 bit D/A converter using Op Amp showing input bit 101. Calculate the theoretical output voltage for same. [6]
- c) Define the terms with respect to PLL [5]
- i) Lock range
 - ii) Capture range
 - iii) Pull-in time
 - iv) Free running frequency

OR

- Q8) a)** Draw neat diagram of weighted resistor DAC [8]
- b) Explain the following specification of ADC [6]
- i) Resolution
 - ii) Conversion time
 - iii) Quantization error
- c) Draw diagram of any one application of IC PLL 565 in detail. [2]

