

Total No. of Questions : 4]

SEAT No. :

PC388

[Total No. of Pages : 1

[6359]-508

S.E. (Electrical) (Insem)

ANALOG & DIGITAL ELECTRONICS

(2019 Pattern) (Semester - III) (203143)

Time : 1 Hour]

[Max. Marks : 30

Instructions to the candidates:

- 1) Answer Q1 or Q2, Q3 or Q4.
- 2) Neat diagrams must be drawn wherever necessary.
- 3) Figures to the right indicate full marks.
- 4) Assume suitable data, if necessary.

- Q1)** a) What is SOP form of reduction? Give one example of it with K map. [5]
b) Draw logical diagram of 2:4 decoder. Explain its working with truth table. [5]
c) Minimize the following Boolean function-using K Map.
 $F(A, B, C, D) = \sum m(0, 1, 3, 5, 7, 8, 9, 11, 13, 15)$ [5]

OR

- Q2)** a) What is POS form of reduction? Give one example of it with K map. [5]
b) State at list four Boolean laws. Prove any one of them. [5]
c) With the help of truth table explain the working of 3 bit Full Adder. [5]
- Q3)** a) Give comparison between Combinational Logic Circuit and Sequential Logic Circuit. (Minimum 5 points). [5]
b) Design MOD 04 Asynchronous UP Counter. Also draw timing diagram for the same. [5]
c) With the help of neat diagram explain the working of 3 bit Ring Counter. Draw its timing diagram. [5]

OR

- Q4)** a) Give comparison between Synchronous Counter and Asynchronous Counter. (Minimum 5 points). [5]
b) What is modulus of counter? Draw neat diagram of MOD 08 Synchronous UP counter with its timing diagram. [5]
c) With the help of neat diagram explain the working of 3 bit Twisted Ring Counter. Draw its timing diagram. [5]

