Total No. of Questions : 4]

SEAT No. :

PE-550

[Total No. of Pages : 2

[6578]-23

S.E. (Computer Engineering) (Insem.)

DIGITAL ELECTRONICS AND LOGIC DESIGN

(2019 Pattern) (Semester - III) (210245)

Time : 1 Hour] *[Max. Marks : 30*

Instructions to the candidates:

1) ***Attempt Q1 or Q2, Q3 or Q4.***
2) ***Neat diagram must be drawn wherever necessary.***
3) ***Assume suitable data if necessary.***

Q1) a) Minimize the function in SOP form and also draw the diagram

$f(A,B,C,D) = \sum m(0,2,3,5,6,9,11,15) + d(1,13,14)$ **[5]**

b) Simplify logic equation using Quine Mc Cluskey minimization Technique.

$Y(A,B,C,D) = \sum m\ (0,1,3,7,8,9,11,15)$ **[5]**

c) Obtain the minimal POS expression for the following and also draw the diagram using logic gates.

$F(A,B,C,D) = \pi M(0,1,2,4,5,6,9,11,12,13,14,15)$ **[5]**

OR

Q2) a) Write application of Gray Code. Design 3 bit Binary to Gray code converter **[5]**

b) Minimize the function in SOP form

$f(A,B,C,D) = \sum m(0,1,2,3,6,9,10,13,15)$

Also draw the diagram **[5]**

c) Write in i) sign magnitude form

ii) l's complement form

iii) 2's complement form

a) -112 b) -54 **[5]**

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Q3) a) Design 3 bit BCD to Ex-3 code converter. Draw the diagram. **[5]**

b) Design single digit BCD adder using 4 bit binary adder IC 7483. **[5]**

c) Implement full adder using two 4:1 multiplexer and OR gate **[5]**

OR

Q4) a) Design 2 bit magnitude comparator using gates **[5]**

b) Implement f(A,B,C,D) = $\sum m(0,l,2,4,5,6,7,11,13,15)$ using single 8:1 multiplexer. **[5]**

c) Compare Multiplexer and Demultiplexer, Implement

F1= $\sum m(l,3,4,7)$

F2= $\sum m(3,5,6,7)$ using 3:8 Decoder. **[5]**

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