Total No. of Questions : 10]

SEAT No. :

PE-5722

[Total No. of Pages : 3

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S.E. (Computer/Computer Science & Engineering)

MDM-221 : DIGITAL ELECTRONICS & LOGIC DESIGN

(2024 Pattern) (Semester - III)

Time : 2½ Hours] *[Max. Marks : 70*

Instructions to the candidates :

1) ***Attempt Q.1, or Q.2, Q.3 or Q.4, Q.5 or Q.6, Q.7 or Q.8 and Q.9 or Q.10.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Numeric figures in square brackets [] indicate full marks.***
4) ***Use of electronic pocket calculator is allowed.***
5) ***Assume suitable data, if necessary.***

Q1) a) Simplify and implement following expression using K-Map **[5]**

$Y = \sum m\ (0, 1, 2, 5, 7, 8, 9, 10, 13, 15)$

b) Minimise the following expression and implement using logic gates. **[5]**

$(Y = (A + B + \overline{C})\ (A + \overline{B} + \overline{C})\ (\overline{A} + B + C)\ (\overline{A} + \overline{B} + \overline{C})\ (A + B + C)$

c) Perform the subtraction using 1's Complement and 2's Complement method $(151)_{10} - (76)_{10}$. **[4]**

OR

Q2) a) Derive the POS of the following expression using K-Map and implement using logic gates. **[5]**

$F(A, B, C, D) = \prod M\ (0, 2, 3, 8, 9, 12, 13, 15)$

b) Using Boolean algebra theorems, simplify the following expression and implement using logic gates. **[5]**

$F = (A + B)\ (A + C)\ (\overline{A} + \overline{B})$

c) Differentiate between Signed Magnitude, 1's Complement, and 2's Complement representation. Represent –23 using all three methods. **[4]**

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Q3) a) Explain the working of a 4-bit Binary Adder using IC-7483. Write its features and applications. **[5]**

b) Explain the working of a BCD-to-Excess-3 code converter with truth table and circuit diagram. **[5]**

c) State the difference between half and full adder. **[4]**

OR

Q4) a) Draw and explain 4 bit BCD subtractor using IC-7483. Explain the operation on BCD number 5-7. **[7]**

b) Implement the following Boolean function using 8 : 1 multiplexer **[7]**

$$(\bar{A}\ B\ D) + (\bar{A}\ B\ \bar{D}) + (A\ C\ D) + (\bar{B}\ C\ D) + (\bar{A}\ \bar{C}\ D)$$

Q5) a) Convert the following flip-flops : **[5]**

i) SRtoJK.

ii) JK to T

b) Draw and explain 4-bit asynchronous up-counter using JK flip flop. Also draw the necessary timing diagram. **[5]**

c) With neat diagrams explain the working of the following types of shift registers **[4]**

i) Serial-in, serial-out

ii) Parallel-in, serial-out

OR

Q6) a) Define the term "Excitation Table". Write the excitation tables for SR, JK, D, and T flip-flops and explain their importance. **[5]**

b) Design a Mod-6 asynchronous counter using T-flipflop. **[5]**

c) Differentiate between Combinational Circuit and Sequential Circuit. **[4]**

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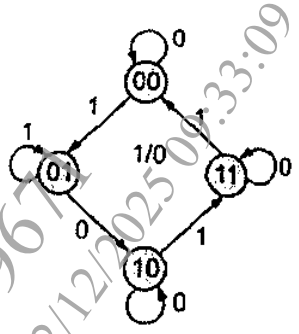
Q7) a) Design a synchronous sequential circuit using JK flipflop for the given state diagram. **[5]**



b) Write a short note on characteristics of logic families. **[5]**

c) Explain the differences between a Finite State Machine (FSM) and an Algorithmic State Machine (ASM) with examples. **[4]**

OR

Q8) a) Explain in detail Mealy and Moore machine **[5]**

i) State diagram and

ii) State table

b) Draw an ASM chart and state table for 2 bit up down counter having mode control input : **[5]**

M=1 : Up counting

M=0 : Down counting

The circuit should generate a output 1 whenever the count becomes minimum or maximum

c) Compare Mealy Machine with Moore Machine **[4]**

Q9) a) Draw and explain the architecture of PLA. **[7]**

b) Explain the difference between PLA, PAL, and ROM in terms of programmability and flexibility. **[7]**

OR

Q10)a) Design a Programmable Logic Array (PLA) to implement the following functions : **[5]**

i) $F1 = \bar{A}B + A\bar{B} + C$

ii) $F2 = \bar{A}\,\bar{B}C + AB$

b) Design BCD to excess-3 code converter and implement it using PAL. **[5]**

c) Write short note on different types of PLD's. **[4]**

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