

Total No. of Questions—8]

[Total No. of Printed Pages—2

Seat No.	
-------------	--

[5668]-184

S.E. (Computer) (I Sem.) EXAMINATION, 2019
COMPUTER ORGANIZATION AND ARCHITECTURE
(2015 PATTERN)

Time : Two Hours

Maximum Marks : 50

- N.B. :-** (i) Neat diagrams must be drawn wherever necessary.
(ii) Figures to the right indicate full marks.
(iii) Use of logarithmic tables, slide rule, Mollier charts, electronic pocket calculator and steam tables is allowed.
(iv) Assume suitable data, if necessary.

1. (a) Explain the following cache updating policies : [6]
(i) Write through
(ii) Write back.
(b) Apply Booth's algorithm to multiply the following numbers. Show every step clearly $(+12) * (-7)$. [6]

Or

2. (a) What is cache coherence ? What are the solutions to cache coherence problem ? Explain any one in detail. [6]
(b) Explain the following : [6]
(i) Direct Mapping
(ii) Associate Mapping.

P.T.O.

3. (a) What are the major functions of I/O module ? [6]
(b) Explain types of instructions according to operations and number of address. Give examples. [6]

Or

4. (a) Explain the following addressing modes with example of each : [6]
(i) Immediate addressing
(ii) Register addressing
(iii) Auto decrement.
(b) List DMA data transfer modes and explain any *one* in detail. [6]

5. (a) Compare superscalar and superpipelined approaches in superscalar processor. [6]
(b) Draw and explain instruction cycle in detail. [7]

Or

6. (a) List and explain various ways in which an instruction pipeline can deal with conditional branch instructions. [7]
(b) Draw and explain the functional block diagram of 8086. [6]

7. (a) Write a control sequence for the following instructions for single bus organization. ADD (R3), R1. Assuming R1 as destination. [7]
(b) Draw and explain micro-programmed control unit design. [6]

Or

8. (a) Differentiate in between Hardwired control and Micro-programmed control. [6]
(b) Draw and explain single bus organization of CPU. [7]